PACKAGING STRUCTURE AND METHOD

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority from U.S. Provisional Application No. 60/188,568, titled "Packaging Structure and Method", filed March 10, 2000. This application is related to commonly assigned copending U.S. Application Atty. Docket No. 60084-300301 titled "Flip Chip Interconnection Structure" and U.S. Application Atty. Docket No. 60084-300101 titled "Flip Chip-in-Leadframe Package and Method"; both said related applications are being filed on the same date as this application, and are hereby incorporated by reference in their entireties herein.

BACKGROUND OF THE INVENTION

[0002] This invention relates to flip chip packaging and, more particularly, to providing a Au/Sn alloy interconnection between a chip and a substrate.

[0003] Conventional methods for interconnecting a flip chip to a substrate include an Anisotropic Conductive Film (ACF) with Ni or Ni/Au coated polymer particles in which a contact type interconnection is made. Fragments of the polymer film which remain trapped at the interconnection point often lead to poor electrical contact and reduced reliability of the package. Additionally, the polymer film reduces the reliability of the bonding interface during the chip bonding process. Conventional flip chip techniques that use either ACF, Non-Conductive Adhesive (NCA) or Non Conductive Polymer (NCP) also suffer from problems in curing the adhesive on adjacent bonding sites on a substrate during the chip bonding process.

[0004] What is needed is a flip chip structure and method that provides for metallurgical interconnection between the flip chip and the substrate and that further provides for improved bonding between the chip and the substrate.

BRIEF SUMMARY OF THE INVENTION

[0005] In one general aspect the invention features a method for providing metallurgic connection between a flip chip and a substrate, by providing a chip having a set of bumps formed on a bump side thereof, providing a substrate having a set of interconnect points on a metallization thereon, providing a measured quantity of a polymer adhesive in a middle region of the chip on the bump side, aligning the chip with the substrate so that the set of bumps aligns with the set of interconnect points, pressing the chip and the substrate toward one another so that a portion of the polymer adhesive contacts the substrate and the bumps contact the interconnect points, and heating the bumps to a temperature sufficiently high to form a metallurgical connection between the bumps and the interconnect points.

[0006] In some embodiments the bumps are stud bumps, and are formed of gold; and the interconnect points include spots of tin, preferably pure tin, on the metallization. In other embodiments the bumps are formed of a metal such as, for example, copper plated with Au or with Ni/Au or electroless Ni/Au; and the interconnect points also may include such materials. In embodiments in which the stud bumps are made of Au and the interconnect points are spots of Sn, the heating step raises the temperature of the bumps sufficiently to create an alloy between the Au and the Sn in a bonding phase at the interface; in preferred embodiments the bonding phase comprises a 80:20 Au:Sn alloy. For such an alloy the bumps may be sufficiently heated by heating the die to a temperature greater than about 200 °C, preferably about 232 °C.

[0007] In some embodiments the method further includes underfilling with a polymer.

[0008] In another general aspect the invention features a chip package structure made according to the method.

[0009] In another general aspect the invention features a chip package structure including a chip having a bumps formed thereon and a substrate having interconnect points on a metallization thereon, the bumps forming contacts with the interconnect points, in which an alloy is formed at an interface between the material of each bump and the material of the interconnect in contact with the bump.

[0010] In some embodiments a cured adhesive polymer is situated in a middle region between the bump surface of the chip and the surface of the substrate.

[0011] In some embodiments the bump material is gold or is a metal such as copper plated with gold or with Ni/Au or with electroless Ni/Au; and the interconnect points also include such materials. In some embodiments the alloy at the interface is an alloy of Au and Sn, and preferably the alloy is a 20:80 Sn:Au alloy.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] Figs. 1A and 1B are diagrammatic sketches in a sectional view showing an illustrative embodiment of stages according to the invention for making a packaging structure according to the invention.

DETAILED DESCRIPTION OF THE INVENTION

[0013] A description of an exemplary embodiment of the invention follows. Using the disclosure herein, substantially conventional apparatus can be modified for use in the process of the invention.

[0014] With reference to the Figs., there are shown in Fig. 1A a chip and a substrate in alignment prior to forming the interconnect according to the invention, and in Fig. 1B a completed interconnect. The flip chip configuration, shown generally at 10, includes a plurality of bumps, e.g. 14, formed on the chip 12, the bumps preferably being gold (Au) stud bumps. The corresponding interconnection points, on a standard substrate 16 metallization are provided with a plurality of preferably pure tin (Sn) spots 18. A central area 20 of the chip on a bump side 22 further includes a spot of adhesive 24 small enough that it does not spread to the gold studs and the interconnection area during a subsequent bonding process. As the chip is connected to the substrate in the flip chip format, the adhesive holds the chip to the substrate and the ends of the stud bumps 14 react with the pure tin spots 18 on the substrate to make metallurgical interconnections 26.

[0015] A substrate strip populated with a row or an array of chips assembled in this manner can be molded using simple tooling, readily adapted from conventional

equipment. The molding preferably provides die underfilling and molding compound along the perimeters of the die simultaneously. Solder balls can then be attached and the completed chips can be singularized by, for example, sawing the substrate.

[0016] The flip chip is aligned with the substrate in such a manner that the gold stud bumps on the chip align with the tin spots on the substrate. After alignment and contact between the Sn spots and the Au stud bumps, the die is heated to a temperature and for a time sufficient to give a metallurgical reaction at the interface between the bumps and the spots, preferably in excess of about 200 °C. For an Au - Sn junction, a suitable temperature the temperature is about 232 °C, and a suitable time is 1 - 2 seconds. At this temperature, the Sn spots melt and the temperature at the bonding interface increases significantly, thereby dissolving some Au from both a metallization layer on the substrate and the stud bumps to create a bonding phase at the interface between the Sn spots and the Au stud bumps. Preferably a 80 %:20 % Au:Sn alloy composition is formed at the interface. Such an alloy provides both reliable electrical contact and advantageous mechanical properties.

[0017] As the Sn/Au interconnection is made the adhesive spot cures to hold the die in space. A subsequent underfilling process of the structure is thereby facilitated as the center region of the chip is already filled with the adhesive polymer. Overmolding fills the remaining space under the die and the space between the chips, resulting in a robust structure.

[0018] An alternative embodiment provides for direct contact between the gold stud bumps and a standard metallization on the substrate. A metallization bond able to withstand the stresses of subsequent processing is thereby formed as there is no interposing polymer at the bonding interface during the chip bonding process.

[0019] To achieve wafer scale packaging, a wafer having stud bumps thereon is placed face up on a heating stage. Substrate pieces, inspected and singulated, with appropriate amounts of adhesive are then picked, aligned, placed and bonded to wafer sites applying conventional process conditions of temperature and pressure. Ultrasonic scrubbing may be employed to clean the substrate site before thermal compression bonding. The disclosed process provides for little waste of substrate material as only particular rejected sites will be discarded, rather than the entire substrate strip.

Additionally, it is not necessary to bond to the rejected dies on the wafer. After fully populating the wafer, the wafer is molded for underfilling and interchip space filling. Dicing the wafer then follows the molding and solder ball mounting steps to singulate the dies.

[0020] In alternative embodiments the stud bumps include Cu plated with Ni and Au, plated Au or electroless Ni/Au, and these materials may be also provided on the bonding sites of the substrate. With the advances in Cu terminal metallurgy, the bonding sites may be finished with Ni and heavy soft Au, thereby providing for interconnections between the wafer and substrate I/Os either by thermal compression bonding utilizing Au or by fusion at low temperatures utilizing Sn like metals to form suitable bonding phases. Once metallurgical contacts are formed, the structure is underfilled and transfer molded simultaneously.

[0021] Other embodiments are within the following claims.